HVCMOS modules for experiments at e^+e^- colliders

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Outlines

- Why HVCMOS?
  - e+e- detector requirements
  - IDEA
  - DMAPS
- ATLASPIX3
  - Single chip characterization
  - Quad modules
  - Serial powering

e+e- Detector Requirements

Physics process		Detector system	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV})\sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} =$ $5 \oplus \frac{10}{p(\mathrm{GeV})\times\sin^{3/2}\theta}(\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	BR(	L L	$\sigma_E^{\mathrm{jet}}/E =$ $3 \sim 4\%$ at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\Delta E/E =$ $\frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$

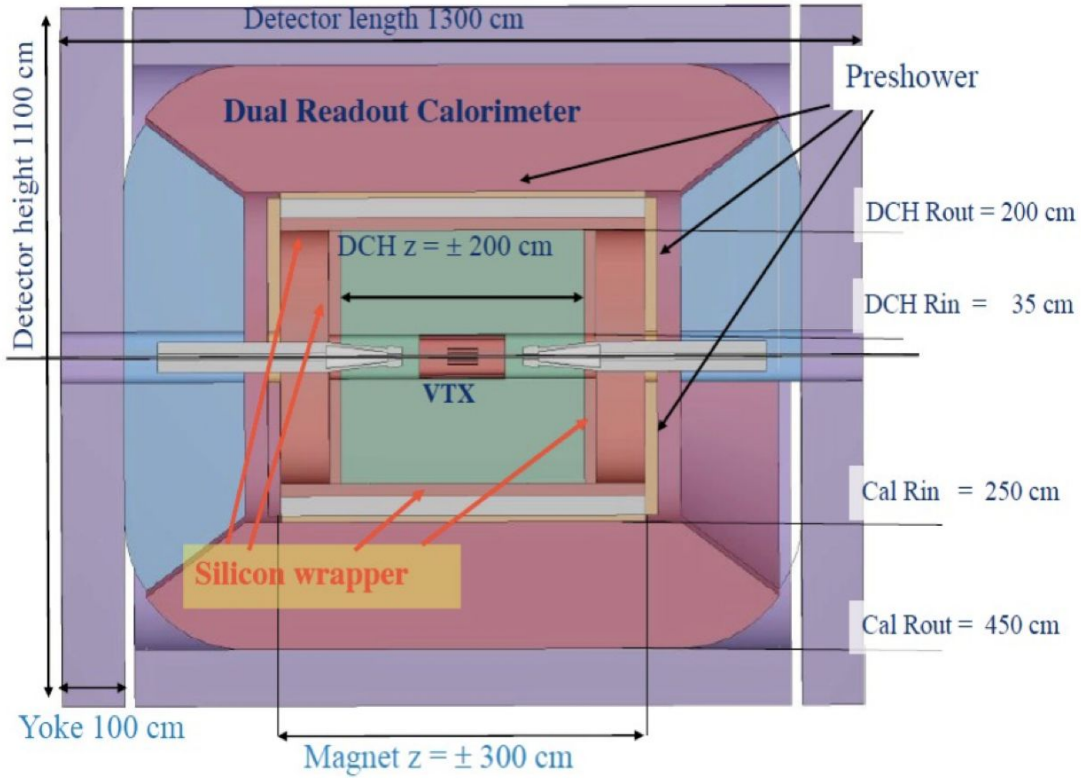
high precision measurements at end of tracking volume

finely segmented vertex detector

challenging requirements on detector material

- Similar approaches for ILC, CLIC, FCCee, CepC:
  - High resolution **pixel vertex detector**
  - Either **full silicon tracker** or **central gas chamber + Si wrapper**

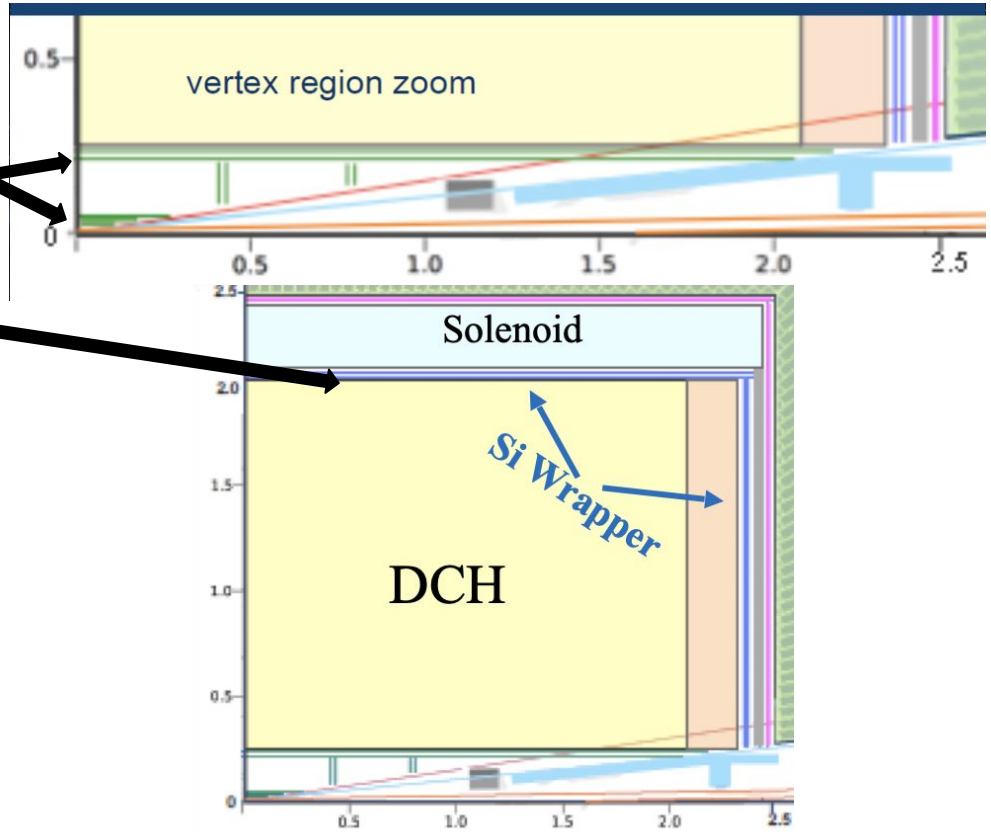
IDEA concept



- **International Detector for Electron-positron Accelerators**
- Central tracking device:
  - light Drift Chamber
- **Silicon detectors for precision measurements**
  - **vertex region**
  - **silicon wrapper**
- Thin solenoid with 2T field
- Dual readout calorimeter
  - supplemented by a pre-shower detector
- Muon chambers in the solenoid return yoke

IDEA - DMAPS (1)

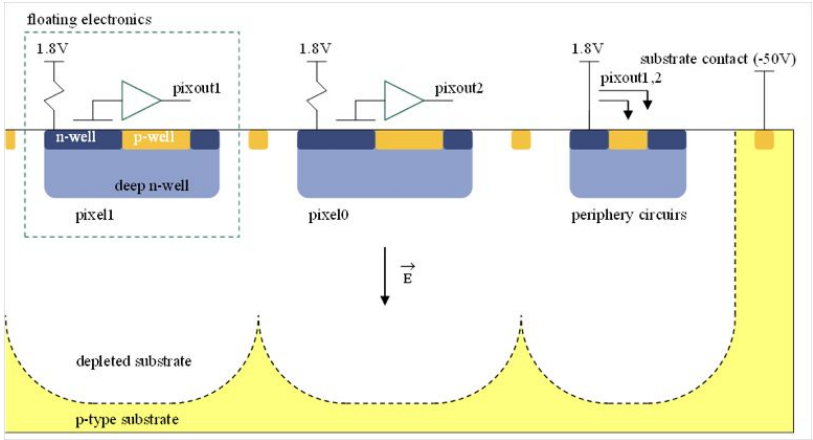
- High precision impact parameter reconstruction with low mass **vertex detector**
- Supplemented by coarser/faster **silicon detectors** in front of the drift chamber
- **Precision silicon layer around central drift chamber**
- **Depleted Monolithic Active Pixels Sensors**
  - CMOS process allows to produce **large areas**, **fast** and **cheap**
  - **no hybridization** (bump-bonding) needed
  - **single detection layer**, can be **thinned** keeping high signal efficiency and low noise rate



IDEA - DMAPS (2)

- High precision impact parameter reconstruction with low mass **vertex detector**
- Supplemented by coarser/faster **silicon detectors** in front of the drift chamber
- **Precision silicon layer around central drift chamber**

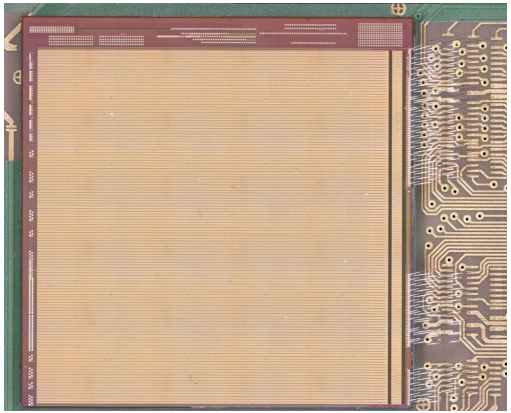
- **D**epleted **M**onolithic **A**ctive **P**ixels **S**ensors
  - CMOS process allows to produce **large areas**, **fast** and **cheap**
  - **no hybridization** (bump-bonding) needed
  - **single detection layer**, can be **thinned** keeping high signal efficiency and low noise rate

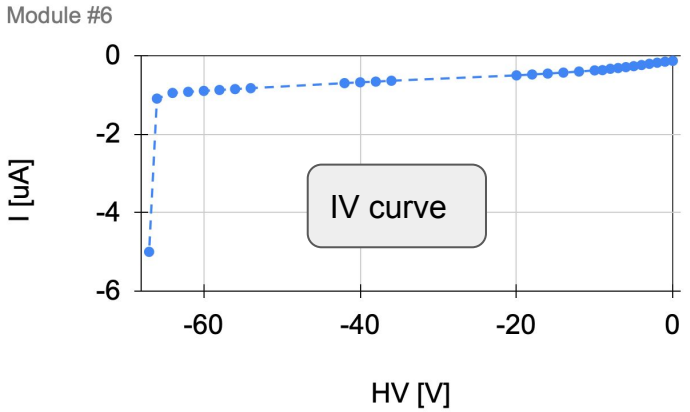


- **Sensor matrix and readout integrated in a single piece of silicon**
- **Pixel electronics embedded in n- and p-wells**
- **Deep n-well** to **isolate** shallow wells from p-type substrate and as **sensor electrode**

ATLASPIX3

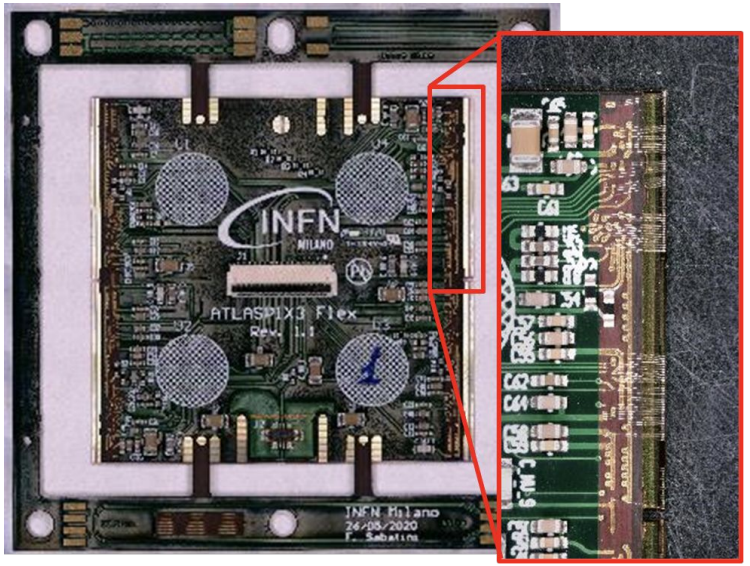
- **ATLASPIX3 features**
  - full-reticle size 20×21 mm² monolithic pixel sensor
  - TSI 180 nm process on 200 Ωcm substrate
  - pixel size 50×150 μm² (25×150 μm² on recent prototypes)
  - breakdown voltage ∼-60 V
  - up to 1.28 Gbps downlink
  - 132 columns of 372 pixels
  - digital part of the matrix located on periphery
  - 25 ns timestamping
  - both **triggerless** and **triggered** readout possible:
    - two End of Column buffers
    - 372 hit buffers for triggerless readout
    - 80 trigger buffers for triggered readout
- **INFN**, **KIT**, **China, UK** collaboration

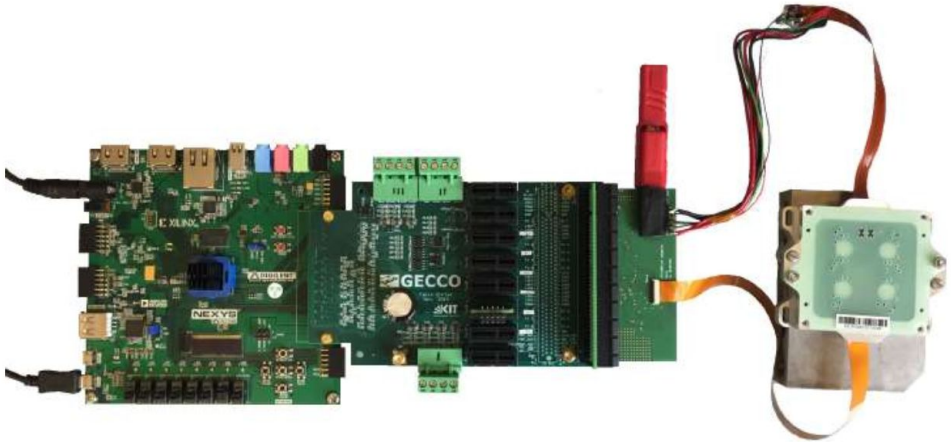




ATLASPIX3 - Quad modules

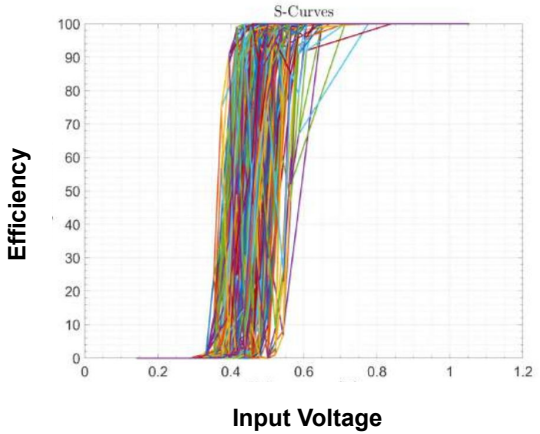
- Multi-chip module assembly
  - aggregates electrical services and connection for multiple sensors
  - **quad module, inspired by ITk pixels**
  - **implemented interface to readout system**
  - **developed software for module calibration**

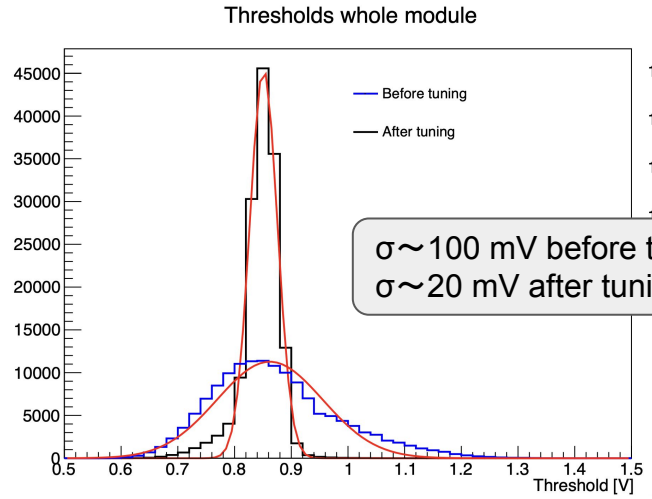




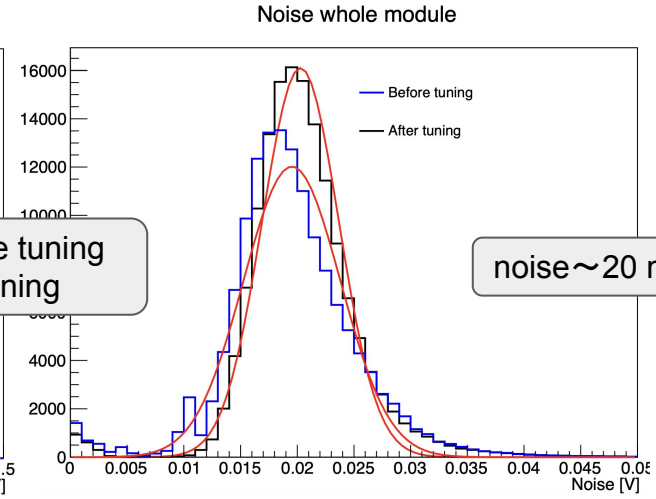
ATLASPIX3 - Threshold and Noise

- **Thresholds** and **noise** measurements
  - **S-Curve** method
  - parameters extrapolated from fit with **Gaussian error function**
- **Thresholds tuning**
  - enhance **uniformity** across matrix
  - tuning circuit **TDAC**





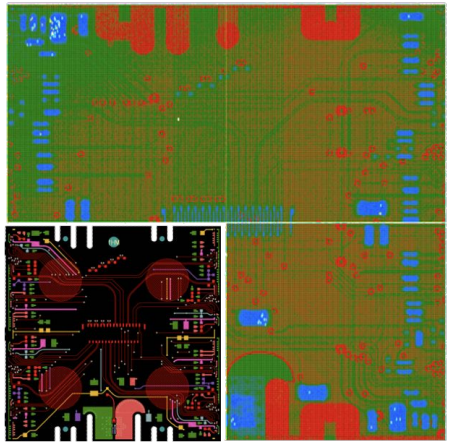
σ∼100 mV before tuning
σ∼20 mV after tuning

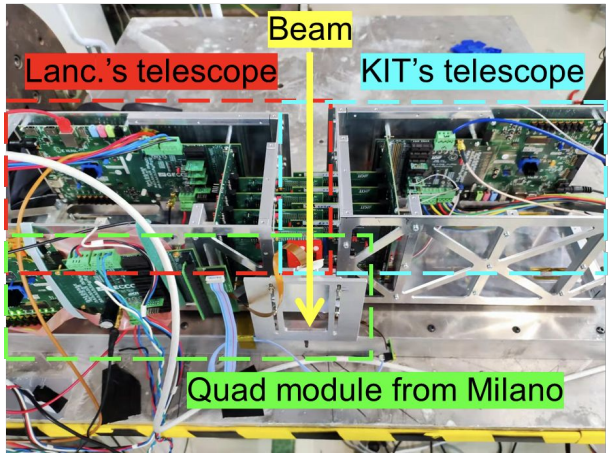


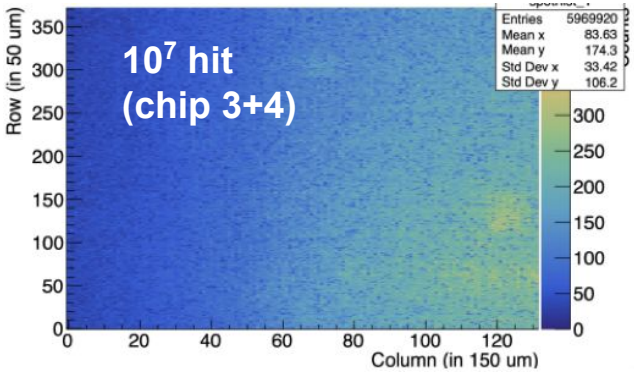
noise∼20 mV

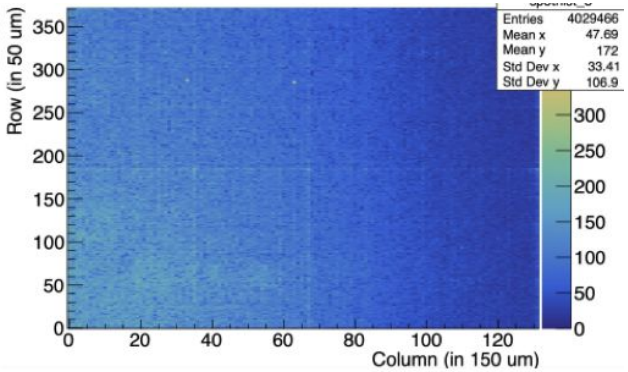
ATLASPIX3 - Operation test

- Amptek Mini-X2 with silver anode, max energy 50 kV
  - Rate range: ~1.5 x 10^4 hits/s to ~ 3.4 x 10^4 hits/s
  - Components on the PCB can be easily identified
- Two modules used for the **testbeam** 4-10 april at **DESY**
  - Module's **operativity demonstrated**



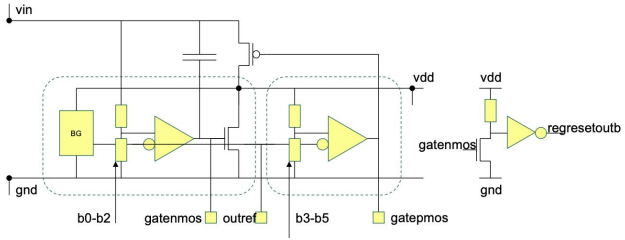


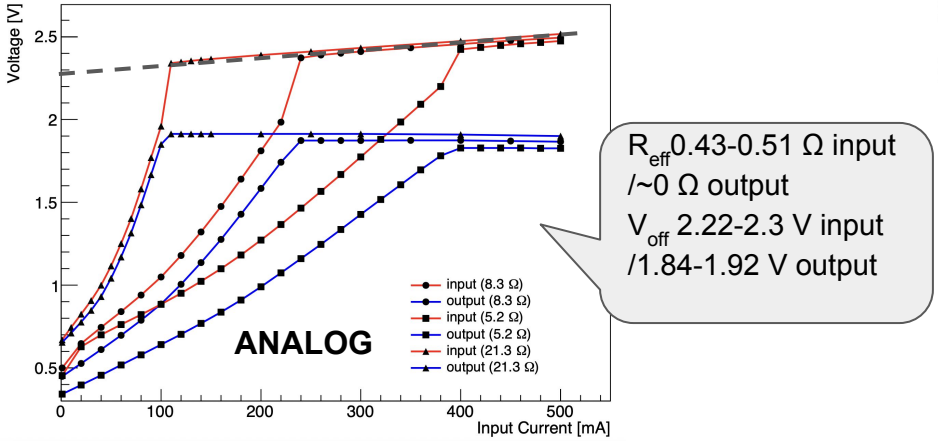




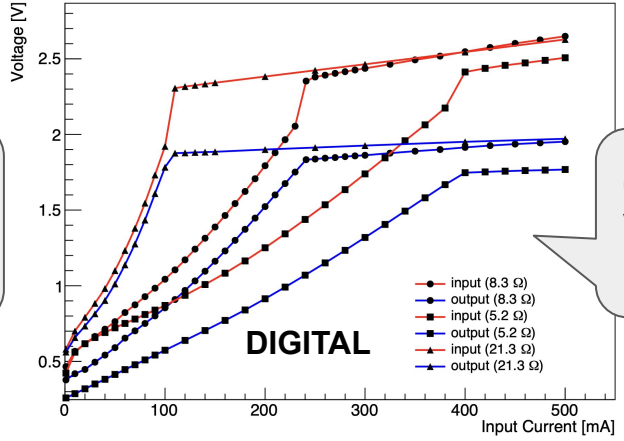
ATLASPIX3 - Serial powering

- Version **ATLASPIX3.1** has possibility for **serial powering** through **two shunt/low dropout regulators**
- Possibility to use a **single power supply for all the 6 alimentation needed to operate the chips**
- **Turn-on curves** (input and output) for digital and analog regulators
- **Different external resistive loads**
- Linear part after the power on fitted with $V_{off}+I*R_{eff}$
- Ideal $R_{eff}\sim 0\ \Omega$, $V_{off}\sim 2$ V for input, ~ 1.8 V for output





R_{eff} 0.43-0.51 Ω input /~0 Ω output
V_{off} 2.22-2.3 V input /1.84-1.92 V output



R_{eff} 0.8-1.1 Ω input/ 0.2-0.5 Ω output
V_{off} 2.05-2.22 V input/ 1.67-1.85 V output

Conclusions and perspectives

- **DMAPS** are **cost effective and performant solution** for the tracking system of next generation e+e- colliders
- **ATLASPIX3** is a **full size detector** providing **most of the features needed by e+e- experiments**
- Deployment on a **real detector system requires the aggregration of data and services**, for this purpose **multi-chip modules have been realized and successfully tested**
- Further integration requires to be able to **chain multiple modules using the same serial-powering concept developed for the silicon trackers for HL-LHC**
- **Early tests on the shunt regulators implemented on the ATLASPIX3.1 chips are encouraging and make possible to proceed to a redesign of a module concept based on serial powering and the building of multi-module chains suitable for CepC and FCCee accelerators**

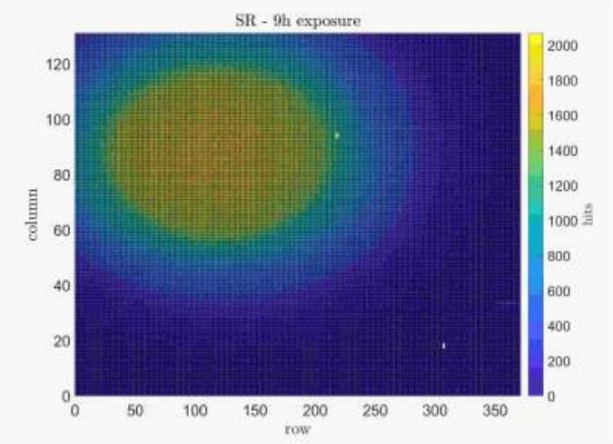
Thanks for your attention!

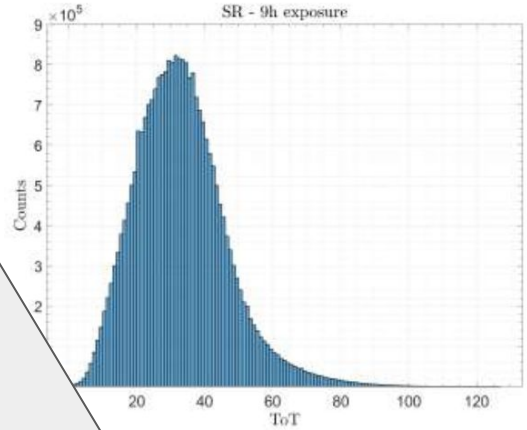
BACKUP

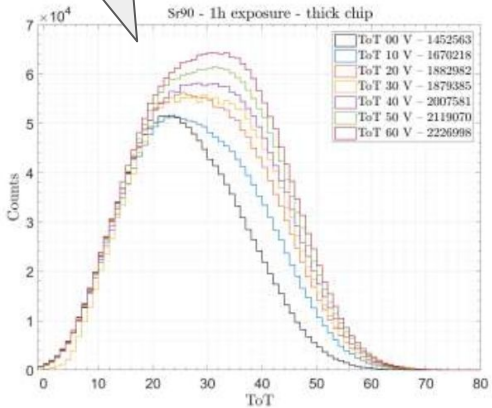
ATLASPIX3 - Radioactive sources

- **Test performance with radioactive sources**
  - ^{90}Sr (2.28 MeV β-rays)
  - ^{241}Am (60 keV γ-rays and 12-22 keV Np L X-rays)

Detection rate for ^{90}Sr with different bias voltages





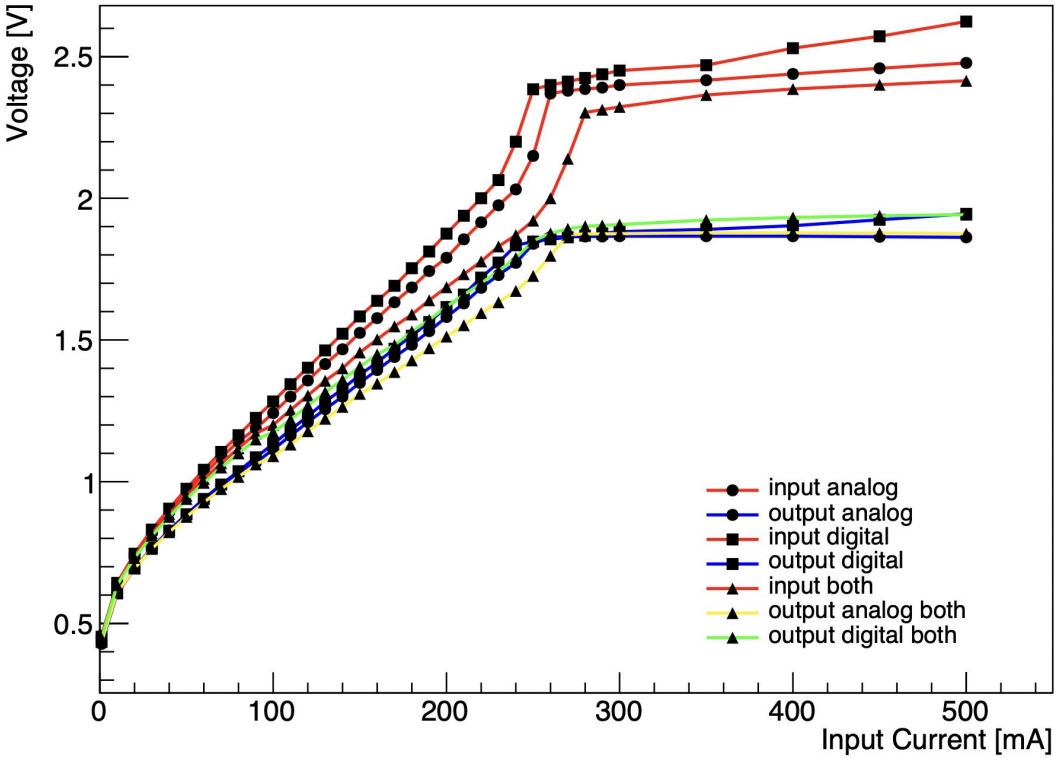


HitMap and TOT for ^{241}Am

ATLASPIX3 - System considerations

- **Complete system consists of 900'000 cm^2 area / 4 cm^2 chip = 225k chips (56k quad-modules)**
  - aggregation of several modules for data and services distribution is essential
  - inner tracker will be 5--10% of this
- **Data rate** constrained by the inner tracker
  - average rate 10^{-4} - 10^{-3} particles cm^{-2} event^{-1} at Z peak
  - assuming 2 hits/particle, 96 bits/hit for ATLASPIX3
  - **640 Mbps link/quad-module** (assuming local module aggregation) provides ample operational margin
  - 16 modules can be arranged into **10 Gbps fast links**: **3.5k links**
    - can also assume 100 Gbps links will be available: 350 links
- **DAQ architecture**
  - **triggerless readout** will fit the data transmission budget but requires off-chip re-ordering of data
  - **triggered readout** will be **simpler** and would also reduce the bandwidth occupancy
- **Power consumption**
  - ATLASPIX3 power consumption **150 mW/cm^2**
  - 600 mW/chip → 2.4 W/module → **total FE power 130 kW**
  - additional power for on detector aggregation and de-randomizations **~2W/link**

ATLASPIX3 - Power consumption



- Full chip turn-on ~300 mA
- Input voltage ~2.3 V
- Power consumption ~690 mW/chip/ ~175 mW/cm^2