Development of a DAQ system for Phase 2 recommissioning of ECAL barrel supermodules

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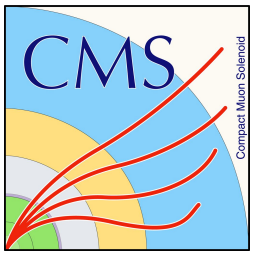
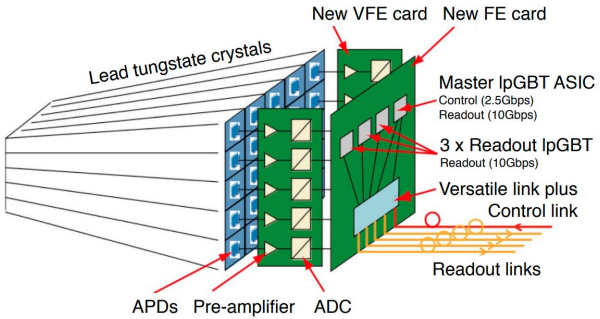
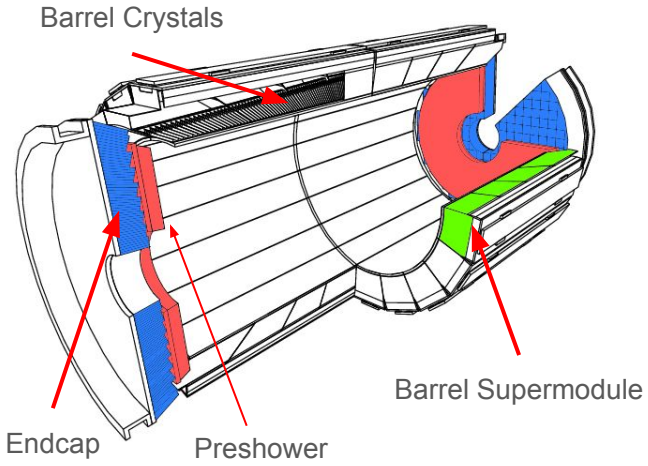


CMS Electromagnetic Calorimeter

- ECAL barrel is composed by 61 200 crystals;
- It measures the energy of particles by collecting the scintillation light produced by crystals;
- The light produced by a 5x5 crystals tower is converted to an electrical signal.
- DAQ system analyses the signal and send it as **trigger-primitive** to the L1 Trigger.

The accelerator upgrade implies a re-examination of the electronics to meet the **new high-luminosity requirements**.





Technical and physics reasons for the EB upgrade

Main goal →maintain the actual physics performance for photons and electrons at HL-LHC.

- New **Level-1 trigger** requirements:
  - increase of the trigger latency to a maximum of 12.5 μs →inclusion of the tracker and HGCal information. The implementation of sophisticated algorithms using machine-learning can now be contemplated.
  - increase of the trigger rate of up to 750 kHz compared to the legacy system;

- **Precision studies** of physics processes → single crystal information provided to L1:
  - reject spike signals (caused by the interaction between APDs and hadrons);
  - precisely match electromagnetic showers to tracks→ reduce backgrounds.

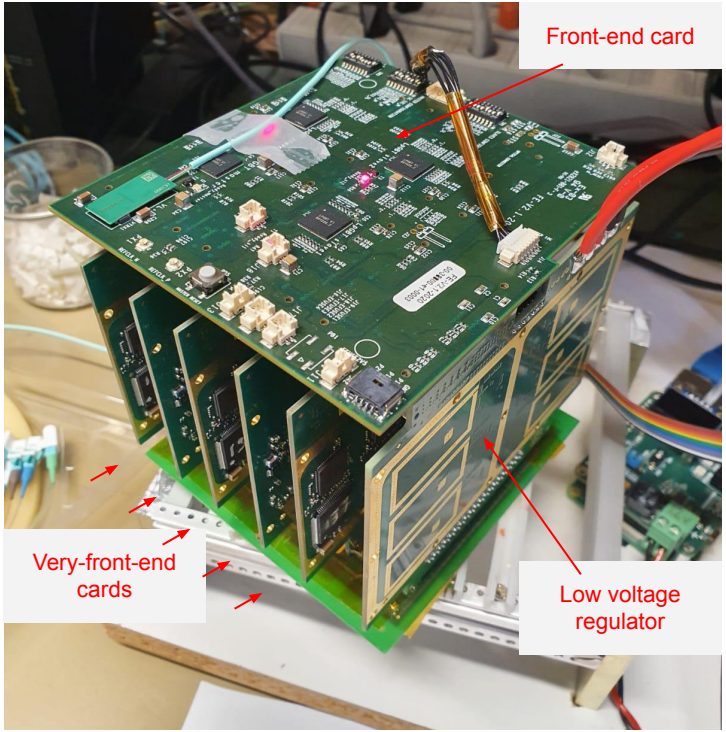
BCP-TT setup

Trigger Tower (TT) prototype:

- reads 25 channels, corresponding to 25 different crystals;
- processes analog signals from crystals and digitizes them;
- sends crystals' APDs data to the BCP.

Barrel Calorimeter Processor (**BCP**) prototype:

- composed by 2 powerful FPGAs;
- analyzes data and transmits trigger primitives to the Level-1 trigger (actually not implemented in the firmware);
- provides the clock (40MHz) and manages the slow control of the TT.



ECAL Upgrade Laboratory in B13, Geneva, CERN

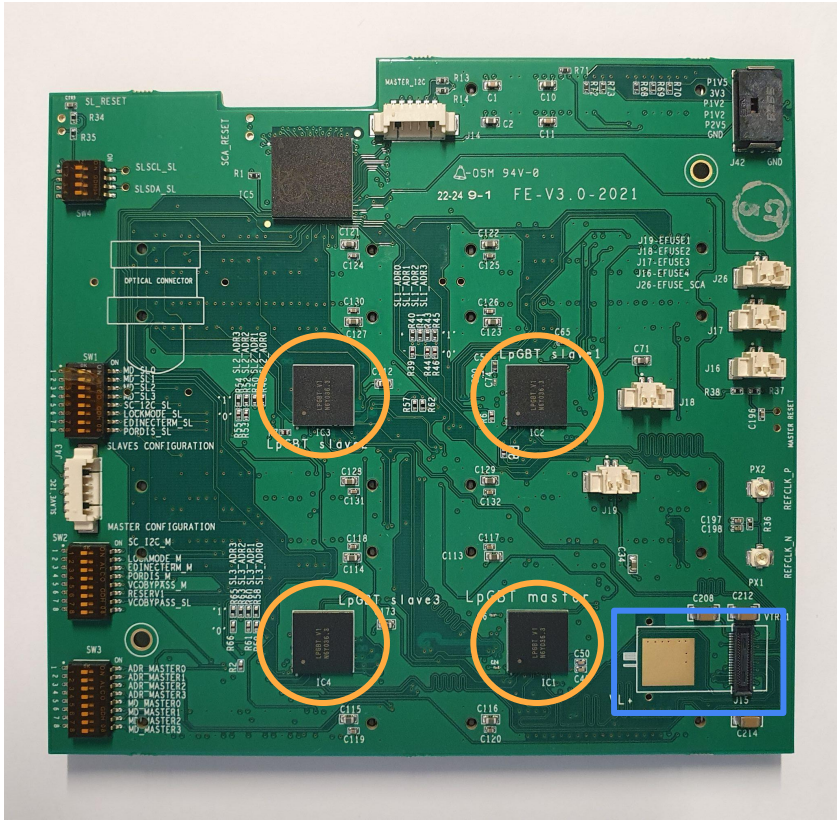
Front-end card

FE card allows the communication between BCP and VFE.

The board is composed of:

- **4 LpGBTs** (Low Power GigaBit Transceiver) → radiation tolerant and **multipurpose ASICs** that allow:
  - data readout;
  - monitoring operations for the whole TT;

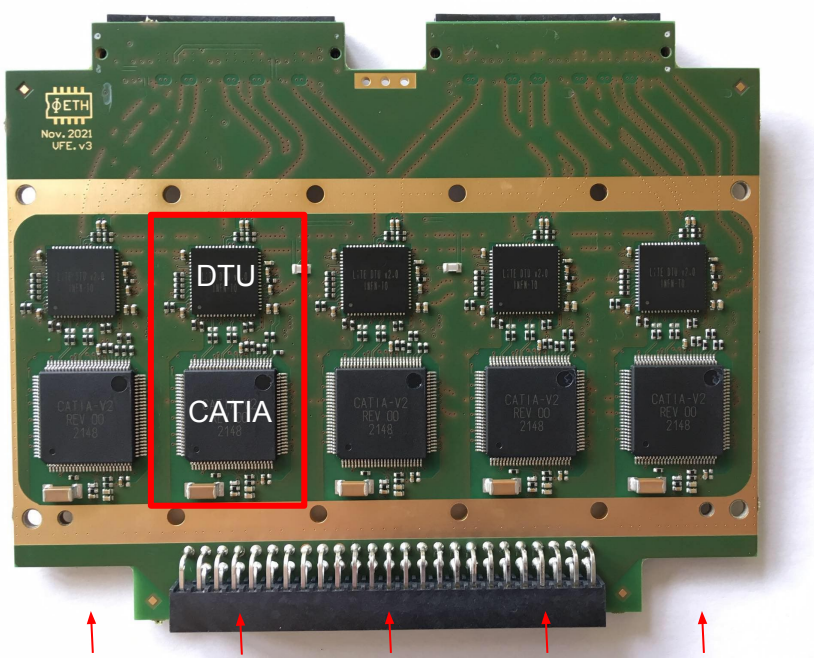
- **1 VTRx** (Versatile Transceiver) → converts LpGBT electrical data in optical signals to send to the BCP and vice-versa.



Very-front-end card

Key point→limit the noise contamination and discriminate anomalous APD signals.

- Reduction of the **signal shaping time** (43→20 ns):
  - reduce the APD leakage current;
  - better discriminate between scintillation and spike signals (interaction APDs - hadrons).
- Dynamic range up to 2 TeV →**2 output gains** used in the amplification process (CATIA)
- The signal is sampled at **160 MHz** during digitization (four times faster respect to the legacy system).

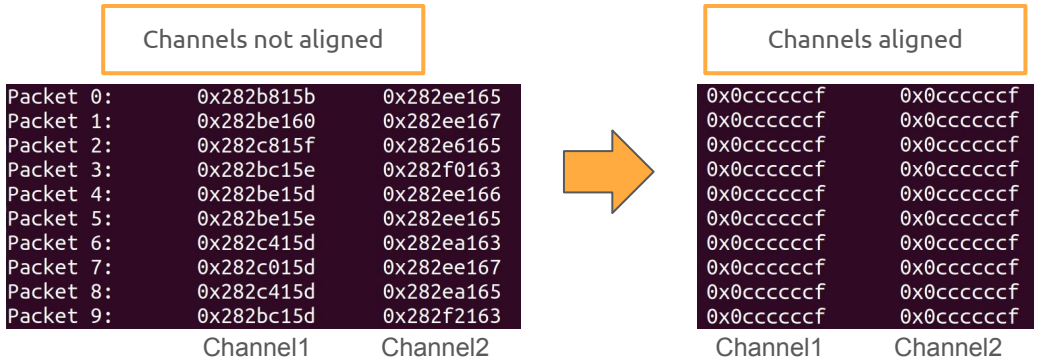


Steps to acquire data (1/4)

1. **Configure all LpGBTs** of the trigger tower to ready state:
   - open 25 e-links per LpGBT → interconnect each device with all 25 channels (1.28 Gb/s e-links);
   - spread 25 clock lines from the master lpGBT to the entire TT;
   - set the LpGBT GPIOs → allow to reset other chips, enable or check the busy-state of a particular VFE channel, check the PLL lock condition;

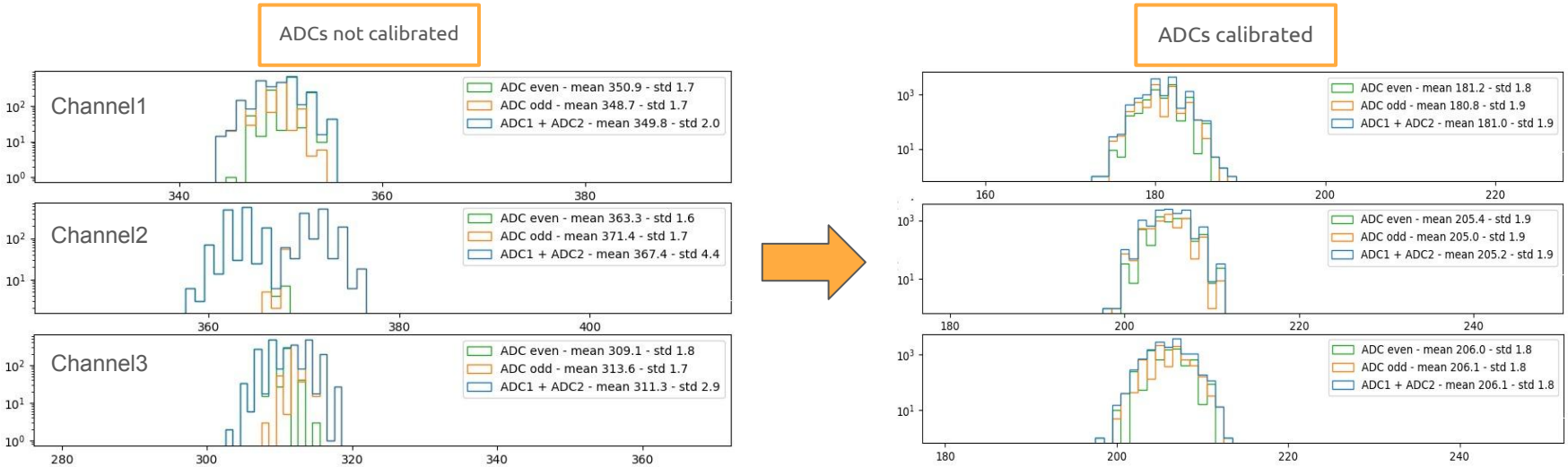
2. Perform the LiTE-DTU **PLL scan** → synchronize LiTE-DTU clock frequency with the BCP;

3. Perform a full automatic **bit alignment of 25 channels** using the Lite-DTU synchronization mode (pattern 0x0ccccccf);



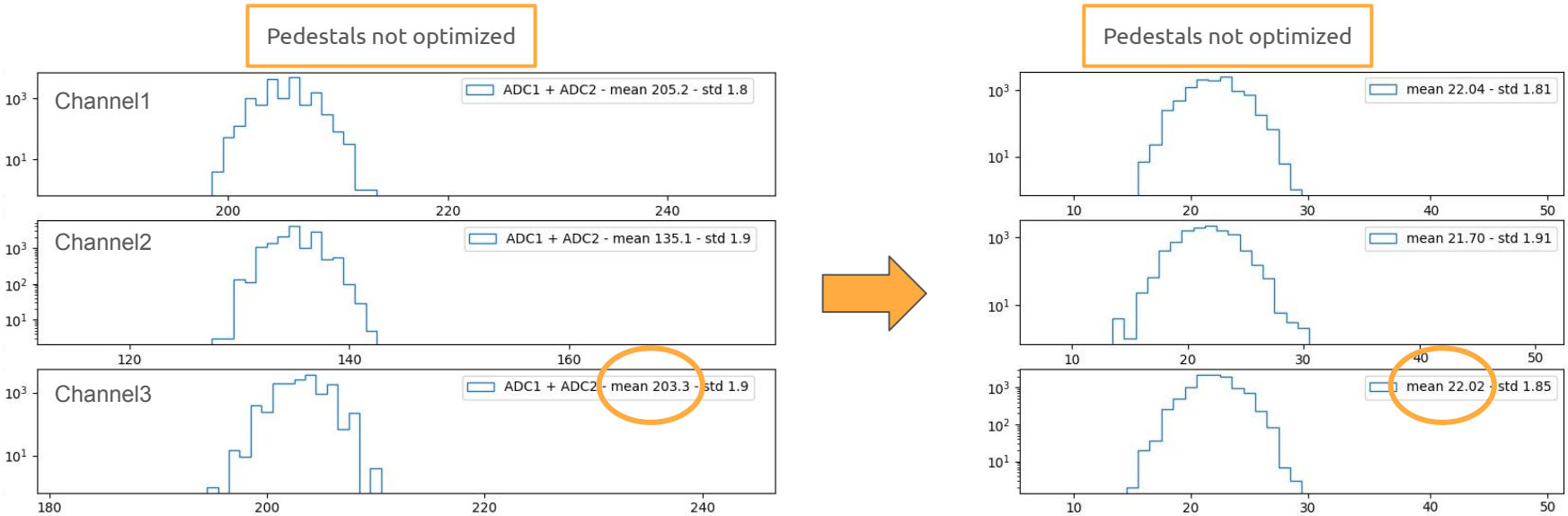
Steps to acquire data (2/4)

4. Since each LiTE-DTU has **two identical ADCs** → ADCs calibration is necessary:
   - set CATIA reference voltage to 1 V;
   - trigger **LiTE_DTU auto calibration** via BCP fast command or via specific register configuration;



Steps to acquire data (3/4)

5. **Optimize pedestals** →center the noise-peak between 10 and 30 ADCs channels;

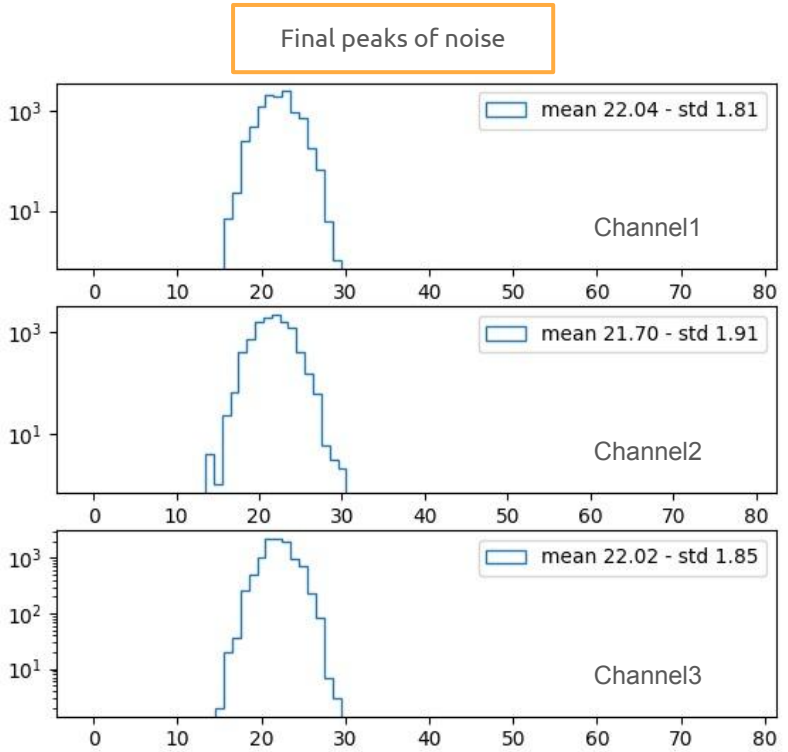


Steps to acquire data (4/4)

6. Data acquisition → **pedestals** and test pulses from VFE devices;
    - good agreement with the expectations;

Next Steps:

- equipping a supermodule with **20 TTs** using the new electronics for multiple BCP acquisition and alignment (2 BCPs will be used for the readout);
- Implementing control and monitoring of the TT through **thermal sensors**;

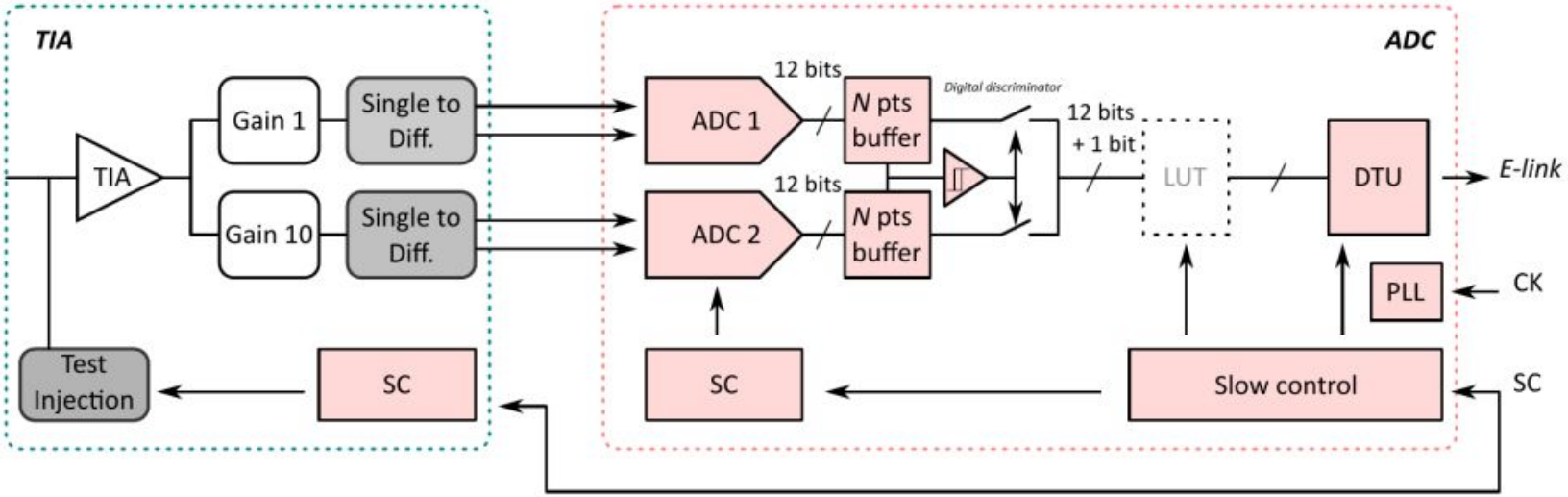


THANK YOU FOR YOUR ATTENTION

BACKUP

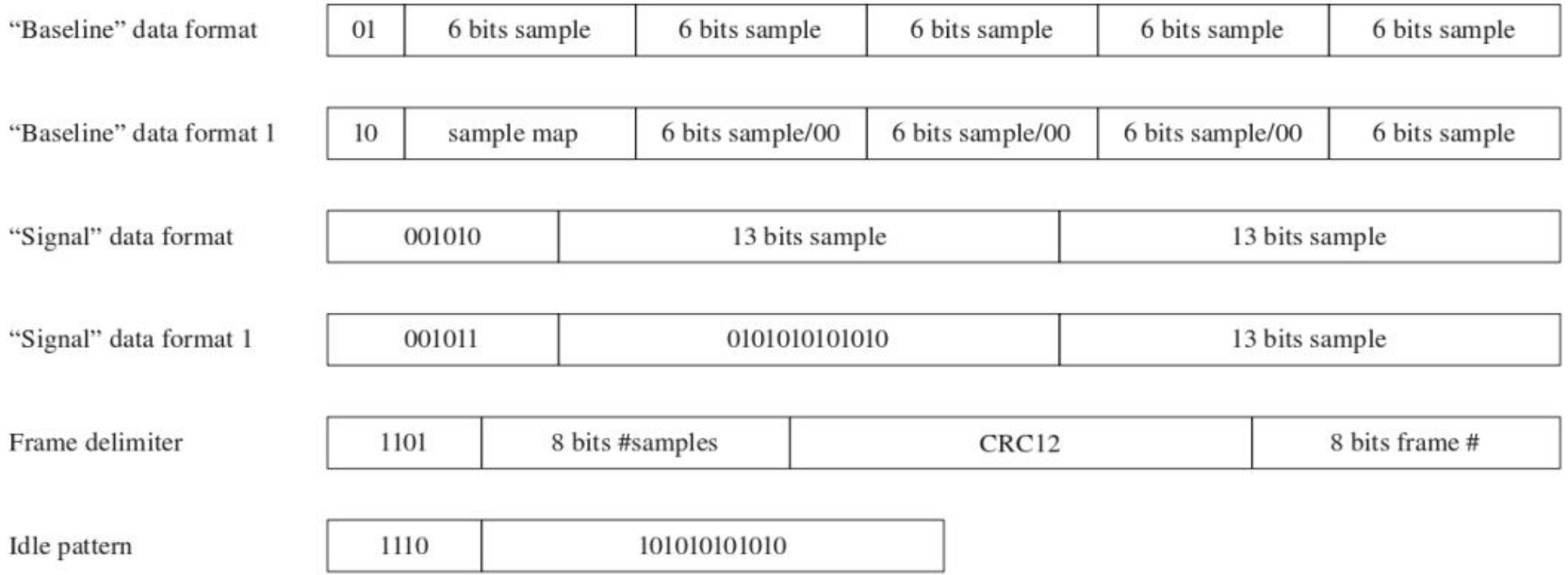
Architecture of the VFE card electronics

- TIA processes the current output of photodiodes to pre-amplify signals from the APDs up to 2 TeV.
- G1 and G10 allow the digitization of each pulse in the chosen dynamic range, using two 12-bit ADCs inside the LiTE-DTU.



Data Format

Every data received have to be transmitted →large volume of data →can be reduced applying an encoding.

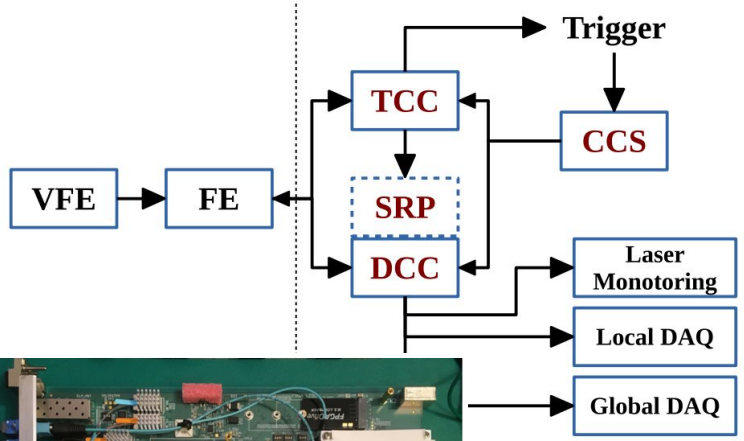


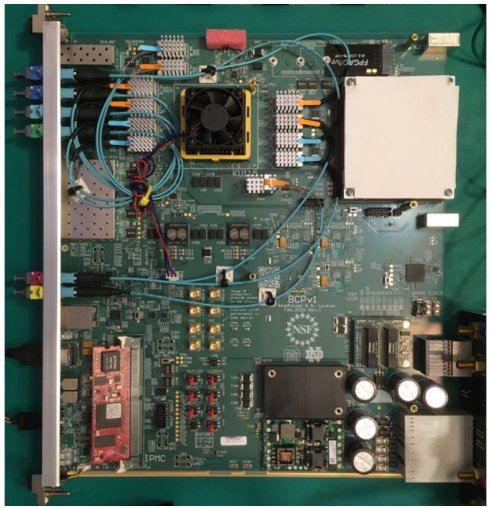
Off-detector electronics (BCP)

The BCP must provide the clock and control to the FE board, and also interface with the DAQ system.

The algorithms required to be implemented in this board include:

- Rejection of anomalous APD signals (spikes);
- Conversion of digitized pulse data into transverse energy (trigger primitives);
- Basic clustering of localised energy;
- Generation of clock and control signals to the FE.





lpGBT ADC calibration

- The ADC measures the value of the input analog positive signal compared to the negative input at reference voltage (V_{ref});
- The master formula to **convert ADC channels to voltage** is the following:

$$ADC(V_{pos}) = 512 \cdot \frac{V_{pos}}{V_{ref}} \cdot Gain + Offset \cdot (1 - \frac{Gain}{2})$$

- *Gain* and *Offset* have to be determined by special measurements in particular conditions:
  - for determining the offset, measuring the ADC response with both inputs at V_{ref};
  - For determining the gain, measuring the ADC channel when the ADC input is grounded (V_{pos} = 0).

VFE temperature measurement

- VFE is equipped of two thermal sensors (**resistors** - Pt1000) able to roughly measure the temperature and prevent overheating:
  - The resistance depends linearly on the temperature;

$$R(t) = R_0 \cdot (1 + \alpha T)$$

- The measure of the VFE temperature is carried out:
  - sending a controlled current I_{bias} generated inside lpGBT-DAC to the resistor;
  - measuring the voltage drop through the calibrated ADC;
  - derive the temperature with the following:

$$T = \frac{1}{\alpha} \cdot \frac{V(t)}{R_0 \cdot I_{bias}}$$