The new readout system for the ALICE Zero Degree Calorimeters in LHC Run 3

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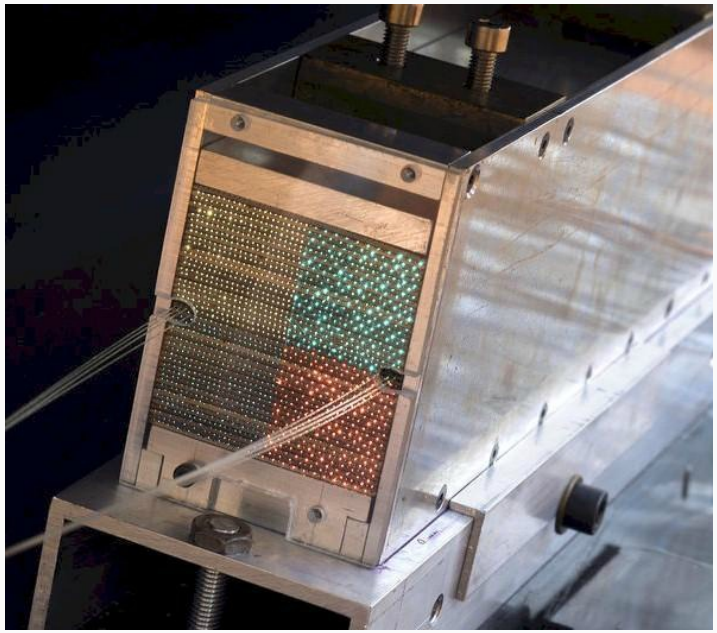
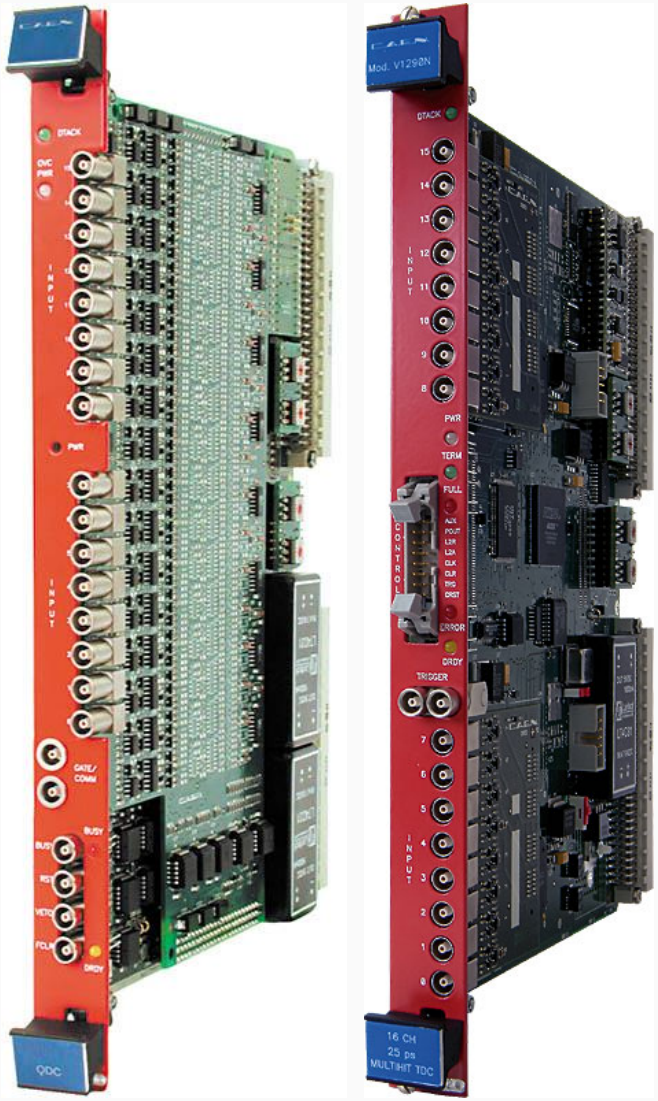
The ALICE Zero Degree Calorimeters



The Zero Degree Calorimeters (ZDC) feature a set of calorimeters placed on both sides of the interaction point, at about 113 m. The purpose is to detect spectator nucleons in order to determine the overlap region in nucleus-nucleus collisions.

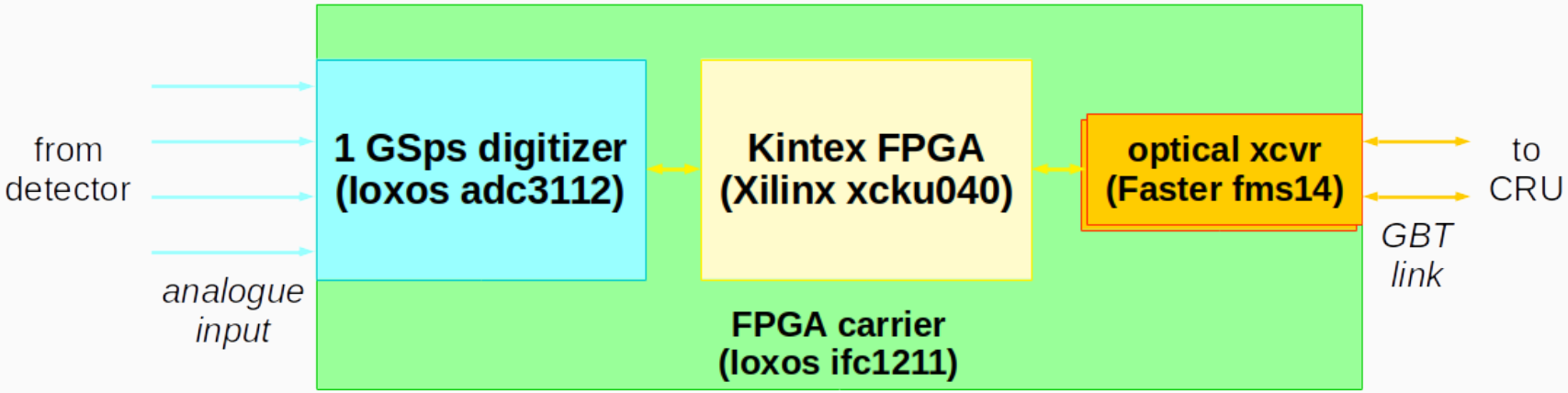
The calorimeters are composed of quartz fibres, arranged inside an absorber made of heavy metal as tungsten or brass. The principle of operation is based on the detection of Cherenkov light produced by the charged particles of the shower in the fibres.

The past readout system for the ALICE ZDC



The readout system was based on custom differential discriminators developed at INFN Torino, commercial QDC (Caen v965) and commercial TDC (Caen v1290).
The problem of this architecture is due to the QDC conversion time of about 10 μs, that limits the event rate (L_0 trigger) around 100 kHz. The current requirement, for Run 3, is the capability to sustain an event rate of roughly 5 M event/s.

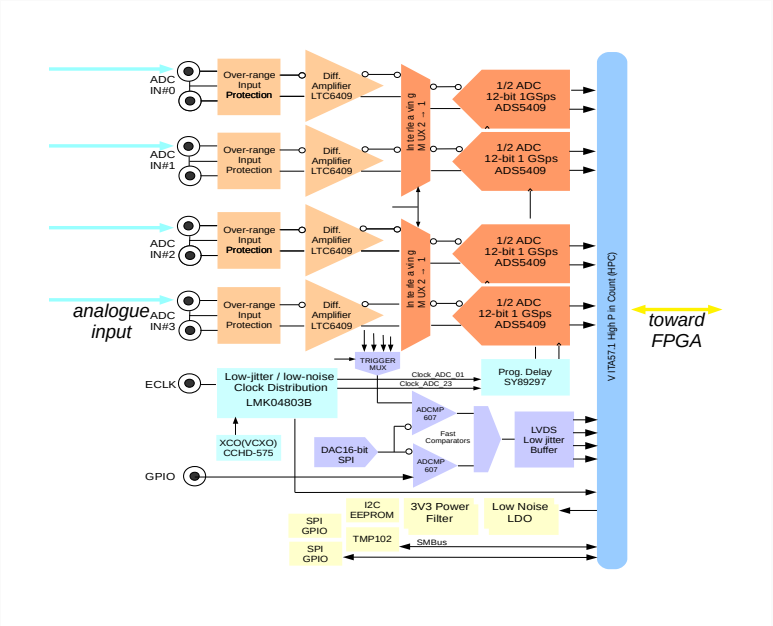
The new readout system for the ALICE ZDC



The new readout architecture is based on an FPGA, to perform data processing and to have a system that can be reconfigured in case of need.

The FPGA is arranged on a VME carrier that host two FPGA Mezzanine Card (FMC) ports. That allows the possibility to add a fast digitizer for the analogue inputs, and an optical transceivers to interface with the DAQ.

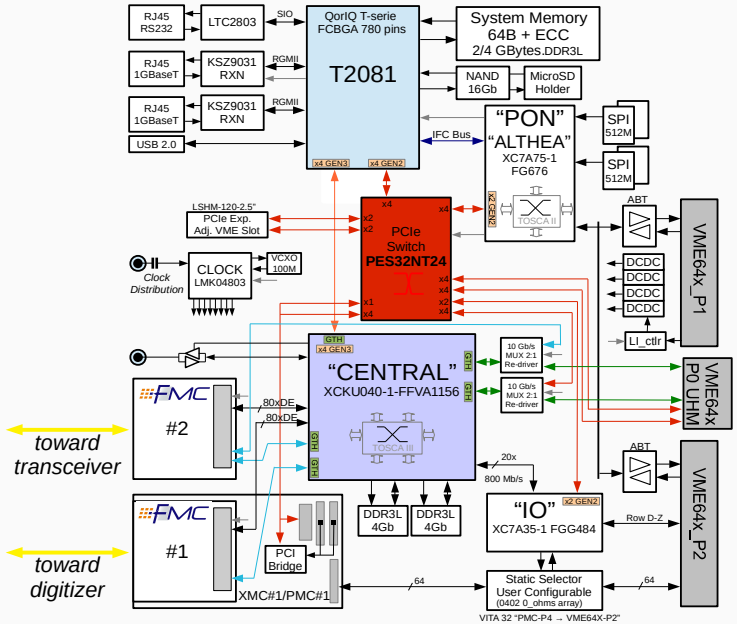
The new fast digitizer



The selected digitizer is the commercial Ioxos adc3112, an FMC module with 4 channels able to run at 1 GSps with a resolution of 12 b, that it is used at the speed of 960 MSps to acquire 24 sample per bunch crossing.

It features a differential DC coupled input, that can also be software configured as single ended with 50 Ω input resistance. The direct coupling is important for the ZDC, since the photomultipliers produce unipolar signals with very large dynamic and the digitizer input range of 1 $\mathrm{V_{pp}}$ is exploited inserting a voltage offset.

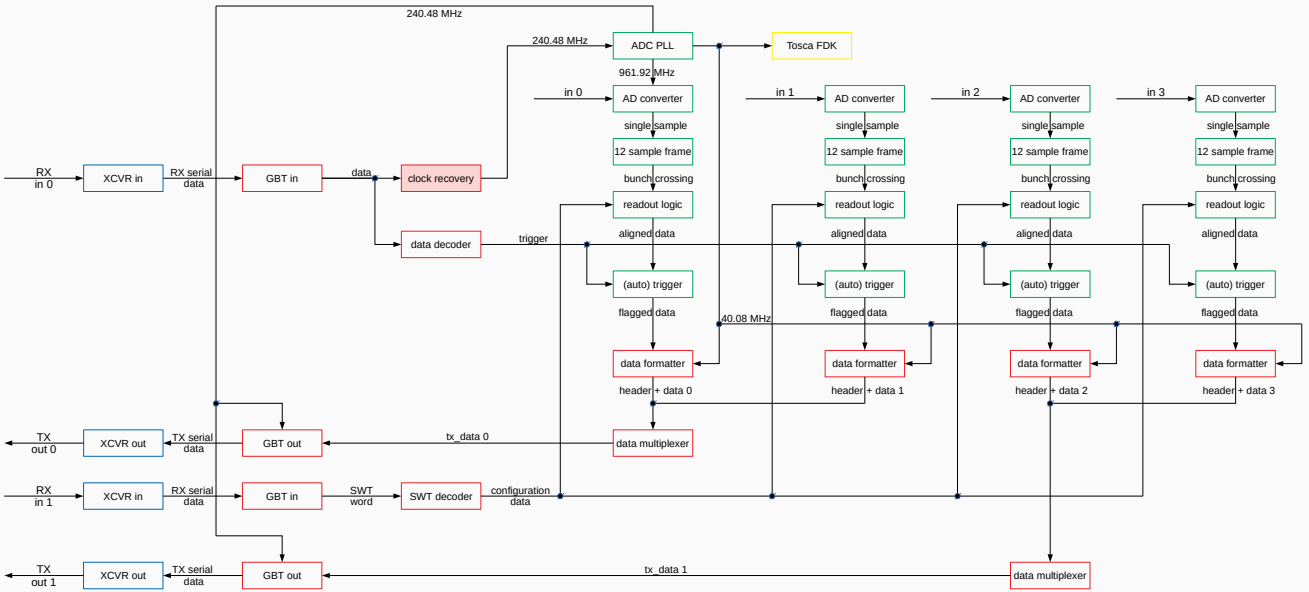
The FPGA carrier with PowerPC processor



The FPGA carrier is the commercial Ioxos ifc1211 that has a 6 U VME format with a PowerPC processor, a Xilinx UltraScale FPGA and many other interface ports among which two FMC.

The very large FPGA is used to perform data processing on the samples coming from the digitizer, with a custom trigger algorithm, and to serialize the information, managing a custom link.

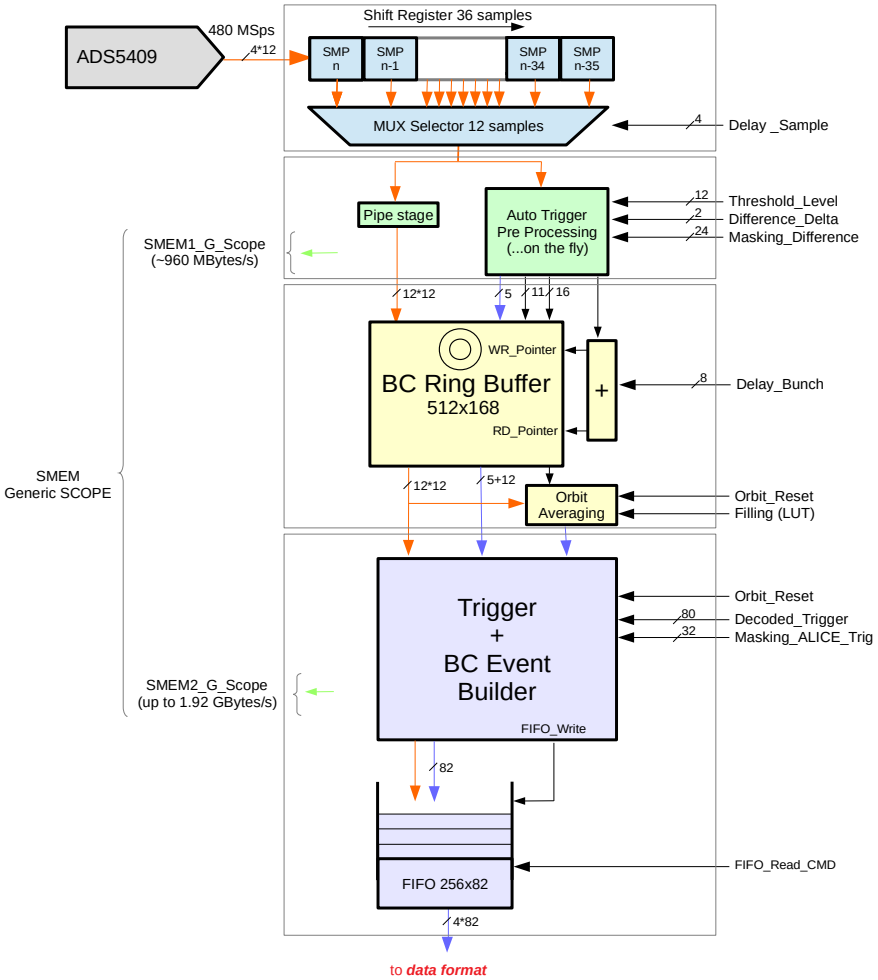
Introduction to the general architecture



The readout firmware, implemented on each FPGA, manages the samples coming from 4 ADC channels. It applies a custom trigger algorithm on each stream and formats the data to be compliant with the GigaBit Transceiver (GBT) protocol.

Beside that, it recovers the timing and clock information from the optical link providing the LHC clock to the whole system, and it decodes the Single Word Transfer (SWT) information to perform the slow control.

Description of the digitizer section



The ADC is configured for applying the 2× decimation filter and the subsequent low pass filter, with the purpose to reduce the total noise and the data rate at the level of 480 MSps.

The digitizer section takes the raw samples coming out from the ADC, and produces a frame of data to format before sending them to the DAQ.

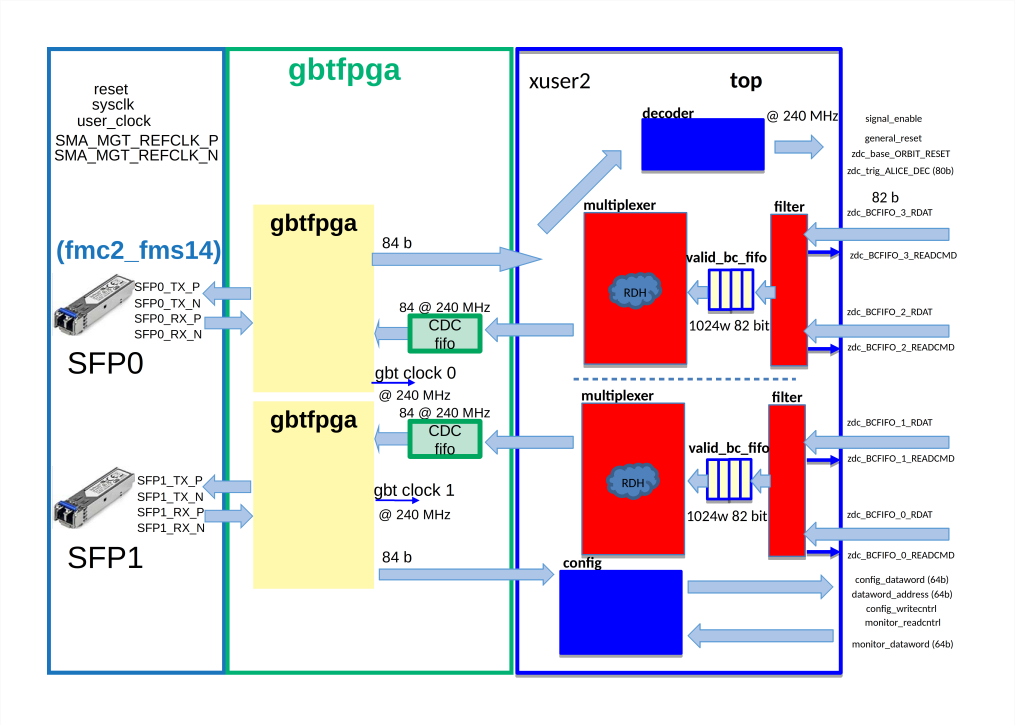
Among other functions, this module aligns the samples in the bunch crossing, applies the auto trigger algorithm and can tag a frame of data with the relevant ALICE trigger information.

Description of the auto trigger algorithm

- Due to the difficulty of the pile up presence, a trigger related to a simple threshold does not fit with the requirement to select events that have a very large dynamics as $1:60$
- So a differential selection is performed with a repeated comparison of close samples with respect to a threshold
  $y_i - y_{i+k} > t \quad \& \quad y_{i+1} - y_{i+k+1} > t \quad \& \quad y_{i+2} - y_{i+k+2} > t$
- With typical waveform shapes and signal timings, the default values are $k = 4$ and $t = 10$
- This means that, considering an ADC input range of $1\ \mathrm{V_{pp}}$ with a $12\ \mathrm{b}$ resolution, the default threshold corresponds about one third of the single neutron energy.

Description of the data formatting section

This entity receives the data path from 4 analog input channels, and makes use of multiplexer blocks to unite these streams towards two serial links.

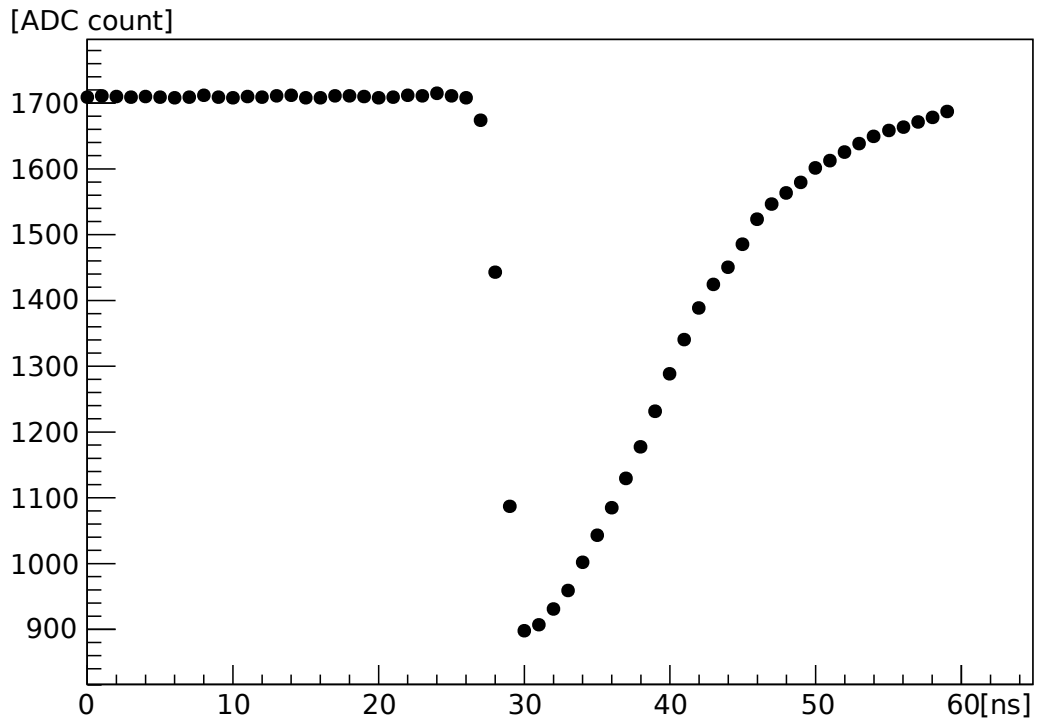


The transmitted data are managed with a different clock from the GBT block, and for that reason a Clock Domain Crossing Fifo was introduced to exchange words between the different clock regions.

The operation and commissioning

Currently the whole system is assembled at CERN, where it is working from this summer, and it is integrated in the DAQ chain complying with all the acquiring modes foreseen in ALICE.

The final commissioning with proton-proton beam of the new readout system is going to be performed in a few weeks, during special runs at low luminosity.



Summary and outlook

- The new readout system of ALICE ZDC detector was developed; it is able to sustain an acquisition rate of 5 $\mathrm{M\ event/s}$
- It is FPGA based, featuring a commercial 1 GSps digitizer with a 12 b resolution from Ioxos, and implements a custom algorithm for auto triggering
- The system, with 26 $\mathrm{channel}$, acquires the neutron and proton calorimeters placed on both sides of the interaction point
- It is working in global acquisition and it is complying with the different acquiring modes foreseen in ALICE; the full integration inside the DCS environment is completed
- The ZDC is expected to be fully operational during the Pb-Pb data taking scheduled for the end of the year, when the ZDC performing features will become crucial